Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A method of controlling data transmission within a memory of a computer system, the computer system comprising a processor, and a memory controller connected to the processor and the memory, the method comprising the following steps:

a) delivering a plurality of data located in a plurality of first memory addresses of the memory to the memory controller; and

b) the memory controller directly storing the plurality of data in a plurality of second memory addresses of the memory instead of transmitting the plurality of data to the processor.

[c2] 2.The method of claim 1 wherein if the first memory addresses are continuous, a source memory address and a bit length of the plurality of data are delivered to the memory controller.

[c3] 3.The method of claim 2 wherein the memory further provides a target memory address so that the memory controller directly stores the plurality of data in the second memory addresses which are continuous.

[c4] 4.The method of claim 2 wherein the memory further provides a plurality of target memory addresses so that the memory controller directly stores the plurality of data in the second memory addresses which are discontinuous.

[c5] 5.The method of claim 1 wherein if the first memory addresses are discontinuous, a first memory address table is provided to the memory controller for receiving the plurality of data.

[c6] 6.The method of claim 5 wherein the first memory address table comprises a plurality of fields, each field comprising a physical memory address, a bit length, and a flag for respectively recording a start address, a bit length, and whether the plurality of data is an end portion with respect to the first memory addresses.

[c7] 7.The method of claim 5 wherein if the second memory addresses are discontinuous, a second memory address table is provided so that the memory controller directly stores the plurality of data in the second memory addresses.

[c8] 8.The method of claim 7 wherein the second memory address table comprises a plurality of fields, each field comprising a physical memory address, a bit length, and

a flag for respectively recording a start addresses, a bit length, and whether the plurality of data is an end portion with respect to the first memory addresses.

[c9] 9.The method of claim 5 wherein if the second memory addresses are continuous, the memory provides a target memory address so that the memory controller directly stores the plurality of data in the second memory addresses.

[c10] 10.A computer system comprising:
a processor for controlling operations of the computer system;
a memory comprising a plurality of first memory addresses and a plurality of second memory addresses; and
a memory controller electrically connected to the processor and the memory, the memory controller having an internal data transmission controller for retrieving a plurality of data according to the first memory addresses, and directly storing the plurality of data in the second memory addresses instead of transmitting the plurality of data to the processor.

[c11] 11.The computer system of claim 10 wherein the memory controller further comprises:
an address register for receiving the first memory ad-

dresses and the second memory addresses; and
a data register for storing the plurality of data.

[c12] 12.The computer system of claim 10 wherein the memory controller is installed in a north bridge circuit.

[c13] 13.The computer system of claim 10 wherein the memory comprises a display memory and a system memory.

[c14] 14.The computer system of claim 13 wherein the first memory addresses are in the display memory and the second memory addresses are in the system memory.

[c15] 15.The computer system of claim 13 wherein the first memory addresses are in the system memory and the second memory addresses are in the display memory.

[c16] 16.The computer system of claim 10 wherein if the first memory addresses are continuous, a source memory address and a bit length of the plurality of data are delivered to the memory controller and at least a target memory address is provided so that the memory controller directly stores the plurality of data in the second memory addresses.

[c17] 17.The computer system of claim 10 wherein if the first memory addresses are discontinuous, a first memory address table is provided to the memory controller for

receiving the plurality of data.

[c18] 18.The computer system of claim 17 wherein the first memory address table is generated by an operating system of the computer system.

[c19] 19.The computer system of claim 17 wherein if the second memory addresses are discontinuous, a second memory address table is provided so that the memory controller directly stores the plurality of data in the second memory addresses.

[c20] 20.The computer system of claim 19 wherein the second memory address table is generated by an operating system of the computer system.